just as it is being sampled. Attention should be paid to the routing of asynchronous signals by separating them and minimizing parallelism.

18.4 ELECTROMAGNETIC INTERFERENCE

Electromagnetic interference (EMI) and crosstalk are closely related topics. It has already been seen that the quality and proximity of a ground plane has a significant impact on a transmission line and the fields that it radiates. Magnetic field strength is proportional to current and is also a function of the loop area defined by the conductors carrying that current. All circuits are loops, because current cannot flow unless a complete loop is formed from the source, through the load, and back to the source. Digital circuits are no exception to this rule, despite inputs typically having high impedance and low DC input currents. A high-speed system moves substantial currents around many individual loops formed by digital buses because of the rapid charging and discharging of transmission lines and input nodes. Even though each bit in a data bus may not be drawn with an explicit return path shown, that return path must exist for the circuit to function.

As the size of the loop formed by the signal's source and return paths increases, that wire radiates a magnetic field of greater strength and is more susceptible to picking up ambient magnetic fields. The general term for a circuit's sensitivity to coupling electromagnetic fields is *EMI susceptibility.* A circuit forms a loop antenna, and a loop antenna is more efficient with increasing area. Loop area and its effect on crosstalk have already been touched on in terms of dielectric height in a PCB. As the signal wire is brought closer to the ground plane, as it is in a lower-impedance design, the loop area and field strength decrease as illustrated in Fig. 18.14.

Minimizing loop area is a key reason why solid ground planes are necessary to high-speed signals. Consider the two scenarios, with and without ground planes, in Fig. 18.15. A ground plane allows a high-speed return current to flow through a path of least inductance that is directly under the signal trace. If the ground plane is replaced by a few discrete wires, those wires cannot lie directly under all signal paths. The return current is forced to take a path that is a greater physical distance from the signal path, with an associated increase in loop area and EMI susceptibility.

Vias along a set of PCB traces can inadvertently create larger loops. When a signal moves between PCB layers, its return current must follow. If a signal changes layers that are on opposite sides of the same ground plane, the return current is able to follow without interruption. Signals often move between layers that do not share the same return plane. In these cases, the return current finds the lowest-impedance path to the return plane that is adjacent to the new signal layer. This path may be direct, capacitive, or a combination of the two. If the new return plane is at the same DC level as the current plane (e.g., two different ground planes), the path of least impedance may be directly through a nearby via that connects the planes. If the new return plane is at a different DC level (e.g., a power plane serves as an AC ground), the return current capacitively couples between planes. Even if the planes share the same DC level, capacitive coupling may be the path of least impedance.

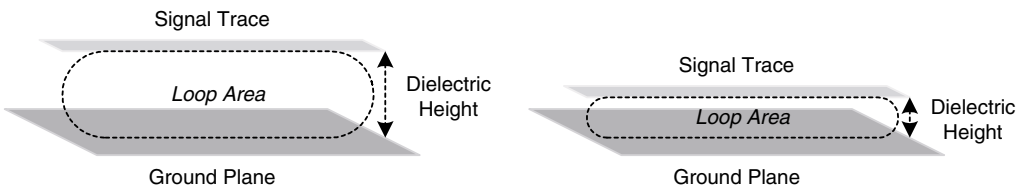

FIGURE 18.14 Loop area vs. PCB dielectric height.

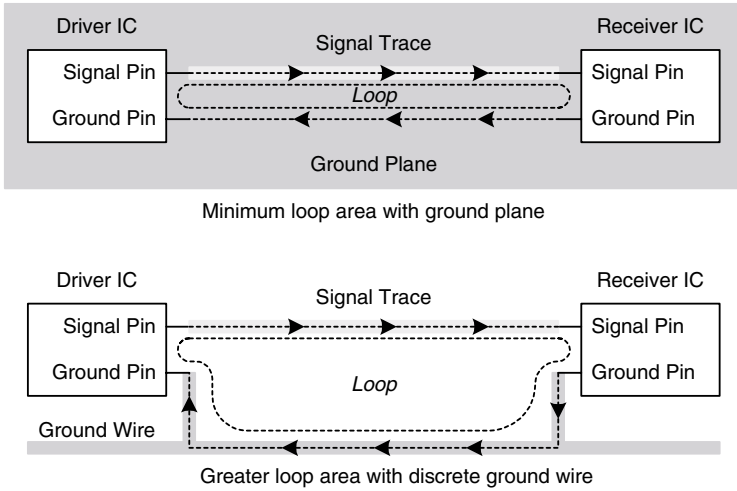

FIGURE 18.15 Greater loop circuit area without ground plane.

Capacitive coupling can occur through bypass capacitors that connect the two return planes and through interplane capacitance that is a function of the PCB dimensions and materials. Low-inductance capacitors are critical to provide adequate high-frequency coupling between planes. Impedance is a product of inductance and frequency. A bypass capacitor's total circuit inductance is the sum of the capacitor's inherent inductance and additional inductance caused by PCB traces and vias that connect it to the return planes. Typical surface mount capacitors in 0603 or similar packages can exhibit total inductance of approximately 2 to 3 nH. This inductance, combined with typical capacitance values of 0.1 or 0.01 μF, allow an impedance calculation at a given frequency. When multiple bypass capacitors are in close proximity to a via, they form a parallel combination with lower total inductance and higher total capacitance—both of which are desirable characteristics. The closer the bypass capacitors are to a via in question, the smaller the loop that is created for high-frequency return current between two planes. Nearby capacitors improve the high-frequency characteristics of the transmission line, whereas more distant capacitors increase the circuit's EMI susceptibility.

Discrete bypass capacitors are often the path of least impedance between return planes. As operating frequencies rise, however, the finite inductance of discrete components becomes more of a problem. A PCB may be constructed with planes separated by very thin dielectrics to provide significant interplane capacitance with negligible inductance. Capacitance increases with decreasing spacing between planes, and inductance decreases with greater surface area that a plane offers. High-frequency systems may require such construction techniques to function properly. These techniques can increase system cost by requiring more expensive thin dielectric materials and a greater number of PCB layers. Such costs are among many complexities involved in creating high-performance systems and must be considered when deciding on the practicality of a design.

The potential for via-induced EMI problems always exists. Conservative designs attempt to route sensitive and very high-speed signals with a minimum number of vias to reduce ground discontinuity problems. When vias are necessary, it is best to switch only between pairs of signal layers that are on opposite sides of the same ground plane.

Return path discontinuities may also be caused by breaks in power and ground planes. A PCB may contain multiple DC voltages (e.g., 5 and 3.3 V) on the same power plane to save money. Dif-